

## **REMARKS**

In the Office Action, the Examiner made the restriction final, withdrew claims 17 – 19 from further consideration, objected to the drawings, rejected claims 16 – 26, 29 and 30 as anticipated by Hsu et al., and rejected claims 27 and 28 as obvious over Hsu in view of Ludikhuize '413. Further art was made of record but not relied upon.

### **Restriction Requirement**

Applicants respectfully disagree with the Examiner's statement that the record does not show how the single inventive concept encompasses all the geometries of the species. Applicants stated in their response that the invention provides a floating guard ring and/or inter-ring zones which have conductivities and/or geometries set so that the free charge carriers are totally depleted when a blocking voltage is applied. Each embodiment illustrated in the drawings is encompassed by this statement, and so it is a single concept. Further, this single concept has not been found in the prior art, and so the single concept is inventive. Thus, the record shows a single inventive concept. Applicants maintain that the election requirement is in error.

In view of the finality of the election requirement, Applicants reserve the right to file a divisional application on the invention of the non-elected claims.

### **Drawing Objection**

The drawing Figure 1 has been amended to add the reference character 10', noted by the Examiner. The specification paragraph referring to the character 10' has been amended as well. Applicants submit that the objection is overcome.

**35 U.S.C. §102(b)**

The semiconductor zones 12, 18 and 19 in Figure 1 of the **Hsu** reference which are stated to be part of an edge structure in the office action are instead part of the drift zone of a lateral MOSFET. The doped regions 14 and 16 form the source and drain regions of the MOSFET and the electrode 26 which is disposed above the semiconductor body forms the gate electrode. Furthermore, the p-doped regions 18 of **Hsu**, in contrast to the invention of claim 1, do not have a ring form. Specifically, the **Hsu** reference teaches islands 18 and regions 19 around the islands 18. These are part of a stripe, according to the teachings of **Hsu**.

Contrary to the Examiner's assertion, there is no reference to a ring in the **Hsu** patent. This feature is found not in the prior art but in Applicants' own disclosure.

The subject-matter of claim 16 is a high voltage resistant edge structure in the edge region of a semiconductor component, with the edge structure comprising at least one inner zone of a first conductivity type and at least one floating guard ring of a second conductivity type arranged in the inner zone. These features are not shown in the **Hsu** reference.

The dependent claims define further inventive features and are also not anticipated by the cited art.

As such, the invention as defined in the claims of the present application is not anticipated by the **Hsu** reference.

**35 U.S.C. §103(a)**

The comments on the **Hsu** reference are incorporated herein from the foregoing section. The reference to **Ludikhuiize** '413 would not lead one of skill in the art to modify

Hsu in a way to achieve the present invention. Ludikhuize teaches a lateral DMOS transistor with a drift region. There is no disclosure of a ring in this reference either.

The present invention as claimed is thus not shown or suggested in the prior art, whether considered alone or in combination, and therefore is a non-obvious improvement thereover.

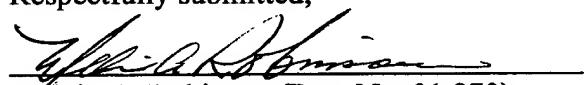
#### **Other Cited Art**

Applicants note the further art cited but not relied upon.

#### **Conclusion**

Each issue raised in the action has been addressed. Early favorable reconsideration and allowance is hereby requested.

Respectfully submitted,

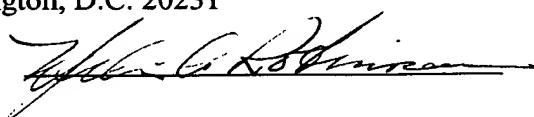
  
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I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to:

The Assistant Commissioner for Patents  
Washington, D.C. 20231

on April 18, 2002.





### **VERSION MARKED TO SHOW CHANGES**

The paragraph beginning on page 7, line 21, has been amended as follows:

In Figure 1, the source zones 9 and the base zones 8 are connected in known fashion to the source electrode 10, and thus to the source terminals S, via contact holes 10' [(not labelled)]. This shunting of the base zone 8 and the source zone 9 makes it possible to keep a parasitic bipolar transistor from being turned on there.